UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,621	03/31/2004	Pierre Busson	361170-1028	5448

32914 7590 08/20/2008

GARDERE WYNNE SEWELL LLP
INTELLECTUAL PROPERTY SECTION
3000 THANKSGIVING TOWER
1601 ELM ST
DALLAS, TX 75201-4761

EXAMINER	
PENG, FRED H	

ART UNIT	PAPER NUMBER
2623	

MAIL DATE	DELIVERY MODE
08/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,621	BUSSON ET AL.	
	Examiner	Art Unit	
	FRED PENG	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-20,23-28,30-41 and 43-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18-20,23-28,30-41 and 43-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 05/05/2008 have been fully considered but they are not persuasive.

Applicant argues on page 16 lines 1-8 of Remarks that it is not prima facie obvious case to fabricate front analog circuitry like tuner except SAW filter and back end digital processing block into one single monolithic substrate.

The Examiner respectfully disagrees with applicant's arguments.

In an analogous art, Tan (NPL ISSCC 98/Paper FP 13.1) discloses integrating front end component analog tuner except SAW filter with post end digital processing block into one single monolithic substrate (FIG.7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined components of Tomasz and Keate to fabricate front end component analog tuner except SAW filter with post end digital processing block into one single monolithic substrate, as taught by Tan to realize the maximum integration benefits.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 4 and 7-10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 5 and 8-11 of U.S. Patent No. 10819086. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Regarding Claim 1, the claimed features are all included in the claim 1 of the co-pending application 10819086 except using the SAW filter placed outside the chip instead of BAW filter inside the chip.

The Official Notice is taken that it is well known in the art to apply SAW filter as bandpass filter and is prohibited to be integrated on a chip.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the BAW with conventional SAW for its availability and good performance.

Claims 4, 7-10 dependent on Claim 1 are also double patenting from Claims 5, 8-11 of the co-pending application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-16, 18-20, 23-28, 30-41 and 43-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz (US 6,400,416) in view of Keate et al (US 5,953,636) and Tan et al (NPL ISSCC 98/Paper FP 13.1).

Regarding Claim 1, Tomasz discloses an electronic component (FIG.3), comprising: an integrated circuit embodied on a monolithic substrate (Col 1 lines 6-8) and comprising:

a tuning module of the zero intermediate frequency dual upconversion (222; Col 3 lines 27-31) then downconversion (240; Col 3 lines 47-50) type possessing an input that receives a digital terrestrial or cable television analog signal composed of several channels (Cable band input 50-850 MHz);

a bandpass filter (210) disposed between frequency transposition stages and delivering a filtered analog signal containing the information conveyed by a desired channel and adjacent channels information and can be implemented with or separate from the integrated circuit (Col 3 lines 11-14, 31-33; Col 4 lines 51-54);

a baseband filtering stage (254) disposed on two quadrature output paths of a second frequency transposition stage for performing a first filtering of the adjacent channels information.

Tomasz discloses a bandpass filter (210) but not specifically a SAW filter of the tuning module for this component.

The Official Notice is taken that it is well known in the art to use a SAW filter as a bandpass filter for a upconversion stage and must be separated from a chip.

Tomasz discloses a digital signal processor connected to the tuner integrated circuit with a multibit analog/digital conversion stage linked to the output of the baseband filtering stage and a digital processing block comprising a stage for correcting defects in phase-and amplitude-pairing of the two quadrature paths (Col 6 lines 21-27; Col 5 lines 16-24).

However, Tomasz does not specifically disclose a channel decoding digital module (DM), linked to the output of the defects correcting stage, and comprising a demodulation stage, a digital filtering stage for eliminating the said adjacent channels information, and an error correcting stage for delivering a stream of data packets corresponding to the information conveyed by the desired channel.

In an analogous art, Keate discloses a channel decoding digital module (DM), linked to the output of the defects correcting stage, and comprising a demodulation stage (FIG.3, element 40), a digital filtering stage for eliminating the said adjacent channels information (FIG.3, element

48), and an error correcting stage for delivering a stream of data packets corresponding to the information conveyed by the desired channel (FIG.3, elements 42, 46).

Keate is not explicit about fabrication of all circuitry except SAW filter on a single monolithic substrate.

In an analogous art, Tan further discloses integrating front end component analog tuner with post end digital processing component into one single monolithic substrate (FIG.7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tomasz's component to include post front end processing circuitry integrated on a single substrate, as taught by Keate and Tan to realize the maximum integration benefits.

Regarding Claims 2 and 3, Tomasz further discloses the first frequency transposition stage is able to receive a first transposition signal having a frequency equal either to the sum of the frequency of the desired channel and of a first transposition frequency greater than the upper limit of the said frequency span (Col 3 lines 27-34), or the difference between the said first transposition frequency and the frequency of the desired channel, and wherein the second frequency transposition stage is able to receive a second transposition signal having the said first transposition frequency (Col 3 lines 41-46; down converted to baseband indicating a second transposition signal having the said first transposition frequency).

Tomasz discloses broadly filtering the intermediate frequency signal and leaving the main filtering at the baseband stage (Col 4 lines 55-58) with the bandwidth about half-width of a channel (Col 6 lines 1-4) but not specifically the order of two to three times the frequency width of a channel for Intermediate stage, and around 20% greater than the frequency half-width of a channel for the baseband.

Official Notice is taken that it is well known in the art to design a circuit based on common/standard design practice or individual design goal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tomasz's component to include a 20 MHz bandwidth for IF stage and 20% extra

bandwidth for baseband stage to accommodate a more common IF design practice and relax design specification for baseband for easier implementation.

Regarding Claim 4, Tomasz discloses dual ADC for I/Q stage output, but not specifically discloses the resolution is greater than or equal to 4 bits.

Official Notice is taken that it is well known in the art to use 4 bits or greater resolution for I/Q output as a standard practice.

Regarding Claims 5 and 6, Tomasz and Keate both are silent about the sampling frequency of the analog/digital conversion stage is greater than around 2.5 or 10 times the upper cutoff frequency of the baseband filtering stage.

Official Notice is taken that it is well known in the art to sample at least two times of bandwidth.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to sample the analog/digital conversion stage with minimum 2 times of the bandwidth based on the design requirement.

Regarding Claim 7, Tomasz discloses the cut-off frequency of the digital filtering stage is equal to a frequency half-width of a channel (Col 6 lines 1-3; bandwidth of low pass filter for each I/Q channel is the same as digital filtering stage).

Regarding Claim 8, Tomasz and Keate are silent about a grounding metal plate glued to a rear face of the substrate by a conducting glue.

Official Notice is taken that it is well known in the art to use a grounding metal plate glued to a rear face of the substrate by a conducting glue to relieve the heat dissipation because of the scale of integration.

Regarding Claim 9, Applicant admits the processing method of the substrate is so called "triple well" and is well known in the semiconductor industry (Specification page 7 Para 26).

Regarding Claim 10, Tomasz further discloses the component is a receiver of digital terrestrial or cable television signals (FIG.3).

Regarding Claims 11 and 12, Tomasz discloses a device (FIG.3) comprising:

a surface acoustic wave filter (210; Col 3 lines 11-14; SAW can be used if needed); and

an integrated circuit comprising a monolithic substrate in which the following circuit components are provided:

an input receiving an analog signal including a plurality of channels (Cable band input 50-850 MHz);

a upconversion device to upconvert the received analog signal (222);

a first port connected to an input of the surface acoustic wave filter and coupled to receive the upconverted analog signal for application thereto;

a second port connected to an output of the surface acoustic wave filter to receive a filtered upconverted signal therefrom; wherein first and second ports carrying signals off and on the device (210); and

a downconversion device to downconvert the filtered upconverted signal to an analog downconverted signal centered at zero frequency (240).

a baseband filtering circuit that filters the baseband signal to generate a filtered analog baseband signal; an analog-to-digital converter circuit that converts the filtered analog baseband signal to a digital baseband signal (Col 6 lines 21-27; Col 5 lines 16-24).

Tomasz is not explicit about a digital baseband filtering stage that filters the digital baseband signal to generate a filtered digital baseband signal.

In an analogous art, Keate discloses a digital filtering stage for eliminating the said adjacent channels information (FIG.3, element 48) and Tan further discloses integrating front end

component analog tuner with post end digital processing component into one single monolithic substrate (FIG.7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tomasz's component to include post front end processing circuitry integrated on a single substrate, as taught by Keate and Tan to realize the maximum integration benefits.

Regarding Claims 13 and 32, Tomasz further discloses the upconversion device and downconversion device comprises a zero intermediate frequency dual conversion tuner (Col 5 lines 6-15).

Regarding Claims 14, 33 and 44, Tomasz further discloses the channels of the analog signal extend over a frequency span and wherein the upconversion device upconverts the received analog signal to a frequency that is higher than an upper limit of the frequency span (Col 4 lines 10-15).

Regarding Claim 15, Tomasz further discloses the upconversion device upconverts the received analog signal to a frequency that is the sum of a desired channel frequency plus the upper limit of the frequency span (Col 4 lines 15-20).

Regarding Claims 16, 35 and 46, Tomasz further discloses the surface acoustic wave filter is a bandpass filter having a pass band of at least two times a frequency width of a channel in the analog signal (Col 4 lines 58-61; broadly enough indicates at least two times of a channel bandwidth; minimum of two times of the bandwidth is required for the IF stage).

Regarding Claim 18, Tomasz further discloses the filtered upconverted signal includes both signals relating to the selected channel and adjacent channel information, and wherein the baseband filtering circuit performs filtering on the adjacent channel information in the baseband

signal (Col 4 lines 1-4; 3 MHz bandwidth performs filtering on the adjacent channel information in the baseband signal).

Regarding Claim 19, Tomasz further discloses the baseband filtering circuit performs both in phase and quadrature phase filtering of the baseband signal (Col 5 lines 6-15).

Regarding Claims 20, 36 and 47, Tomasz further discloses the baseband filtering circuit is a low pass filter typically having an upper cut-off frequency about half width of a channel (Col 6 lines 1-3) but not slightly greater.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to slightly relax Tomasz's design requirements for easy implementation.

Regarding Claim 23, Tomasz further discloses the filtered upconverted signal includes both signals relating to the selected channel and adjacent channel information, and wherein the digital baseband filtering stage performs filtering on the adjacent channel information in the baseband signal (digital filter is a baseband filter to performs filtering on the adjacent channel information).

Regarding Claims 24, 37 and 48, Tomasz further discloses the digital baseband filtering stage is a low pass filter having an upper cut-off frequency substantially equal to a frequency half width of a channel (Col 6 lines 1-4).

Regarding Claims 25, 38 and 49, Keate further discloses means for decoding the filtered signal and delivering a stream of data packets corresponding to information in a desired channel of the analog signal from the filtered digital baseband signal (FIG.3).

Regarding Claim 26, Tomasz further discloses the device is a receiver of digital terrestrial or cable television signals (FIG.3; 50-860 MHz tuner is a receiver for cable television).

Regarding Claims 27, 31 and 43, Tomasz discloses the analog signal is a cable television signal (FIG.3).

Regarding Claims 28 and 41, Tomasz discloses a circuit (FIG.3) with corresponding method, comprising:

an input receiving an analog signal including a plurality of channels (Cable band input 50-860 MHz);

an upconversion device to upconvert the received analog signal (222);

a first filter that filters the received analog signal and generates a filtered upconverted signal comprising information from a selected one of the channels and adjacent channel information (210);

a downconversion device to downconvert the filtered upconverted signal to an analog downconverted signal centered at zero frequency (240).

a second filter that filters the analog baseband signal and generates a filtered analog baseband signal comprising information from the selected one of the channels and less of the adjacent channel information (254);

a digital-to-analog converter to convert the analog baseband signal to a digital baseband signal (Col 6 lines 21-26).

Keate discloses a third filter that filters the digital baseband signal and generates a filtered digital baseband signal comprising only information from the selected one of the channels (FIG.3, element 48) while Tan further discloses integrating front end component analog tuner with post end digital processing component into one single monolithic substrate (FIG.7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tomasz's component to include post front end processing circuitry integrated on a single substrate, as taught by Keate and Tan to realize the maximum integration benefits.

Regarding Claims 30, 39 and 50, Tomasz further discloses SAW filter is traditionally being used for IF filter and is connected to the integrated circuit as an off-chip component (Col 3 lines 9-14).

Regarding Claims 34 and 45, Tomasz discloses a upconversion technique but not specifically about upconversion of the received analog signal to a frequency that is the sum of the frequency for the selected one of the channels plus the upper limit of the frequency span.

Official Notice is taken that it is well known in the art to upconvert the whole frequency band.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a frequency band upconversion to ease the tuning design.

Regarding Claim 40, Tomasz further discloses the circuit is used in cable television application (FIG.3; 50-850MHz).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRED PENG whose telephone number is (571)270-1147. The examiner can normally be reached on Monday-Friday 09:00-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on (571) 272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Annan Q Shang/
Primary Examiner, Art Unit 2623

Fred Peng
Patent Examiner

Vivek Srivastava
Supervisory Patent Examiner